3. The circuit of claim 1, wherein the second adjustment stage circuit is activated in response to the second voltage being greater than the first voltage.

4. The circuit of claim 1, further comprising a switching transistor coupled to a capacitor and a load at an output terminal of the switching transistor.

5. The circuit of claim 4, further comprising a switching transistor, wherein the first adjustment stage circuit comprises:

a capacitor configured to transform a positive variation of the second voltage into a variation of an intermediate current;

a current source configured to generate a reference current; and

a circuit configured to increase a voltage of a gate of the switching transistor in response to the intermediate current being greater than the reference current.

6. The circuit of claim 4, further comprising a switching transistor, wherein the second adjustment stage circuit comprises:

a capacitor configured to transform a negative variation of the second voltage into a variation of an intermediate current;

a current source configured to generate a reference current; and

a circuit configured to increase a voltage of a gate of a switching transistor in response to the intermediate current being greater than the reference current.

7. The circuit of claim 4, wherein each of the first adjustment stage circuit and the second adjustment stage circuit comprise a p-channel metal oxide semiconductor (pMOS) transistor having:

a source node coupled to a node that carries the larger of the first voltage and the second voltage; and

a drain node coupled to a gate of the switching transistor.

8. A method, comprising:

comparing a first voltage at a first terminal and a second voltage at a second terminal;

determining that the first voltage is greater than the second voltage, and, based thereon, limiting a positive inrush current flowing between the first terminal and the second terminal; and

determining that the second voltage is greater than the first voltage, and, based thereon, limiting a negative inrush current flowing between the first terminal and the second terminal.

9. The method of claim 8, wherein limiting the positive inrush current comprises:

transforming a positive variation of the second voltage into a variation of an intermediate current;

generating a reference current; and

increasing a voltage of a gate of a switching transistor in response to the intermediate current being greater than the reference current.

10. The method of claim 9, wherein the reference current is a current proportional to an absolute temperature.

11. The method of claim 8, wherein limiting the negative inrush current comprises:

transforming a negative variation of the second voltage into a variation of an intermediate current;

generating a reference current; and

increasing a voltage of a gate of a switching transistor in response to the intermediate current being greater than the reference current.

12. The method of claim 11, wherein the reference current is a current proportional to an absolute temperature.

13. The method of claim 8, wherein limiting the positive inrush current comprises generating a selection signal that activates an adjustment stage circuit.

14. The method of claim 8, wherein limiting the negative inrush current comprises generating a selection signal that activates an adjustment stage circuit.

15. A circuit, comprising:

a switching transistor having an input terminal coupled to a first voltage and an output terminal coupled to a second voltage;

a comparator circuit configured to determine a difference between the first voltage and the second voltage; and

a control circuit coupled to the transistor switch and the comparator circuit, the control circuit configured to limit a positive or a negative inrush current flowing between the input terminal and the output terminal of the transistor switch, the control circuit comprising:

a control stage circuit;

a first adjustment stage circuit coupled to the control stage circuit;

a second adjustment stage circuit coupled to the control stage circuit;

a first inverter stage circuit coupled to a gate of the switching transistor; and

a second inverter stage circuit coupled to the gate of the switching transistor.

16. The circuit of claim 15, wherein the control stage circuit is configured to selectively activate the first adjustment stage circuit or the second adjustment stage circuit based on determining a difference between the first voltage and the second voltage.

17. The circuit of claim 15, wherein the first inverter stage circuit comprises a three-state voltage inverter powered by the larger of the first voltage, the second voltage, and ground, wherein the first inverter stage circuit is configured to:

receive a first control signal inverting the gate of the switching transistor; and

receive a second control signal having a first state of enabling an operation of the three-state voltage inverter.

18. The circuit of claim 17, wherein enabling the operation of the three-state voltage inverter, disables the second inverter stage circuit, the first adjustment stage circuit, the second adjustment stage circuit, and the comparator circuit.

19. The circuit of claim 17, wherein the second inverter stage circuit comprises a starved voltage inverter having limited current and powered by the larger of the first voltage and second voltage and ground through a reference current source, wherein the second inverter stage circuit is configured to receive the first control signal inverting the gate of the switching transistor.

20. The circuit of claim 19, wherein the second inverter stage circuit is operational in accordance with the second control signal being in a second state of disabling an operation of the three-state voltage inverter.

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